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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/039,319	11/09/2001	Christopher B. Kocon	90065.141001.17732.6317.0	9637

7590 11/06/2002

Thomas R. FitzGerald, Attorney
Reynolds Arcade Bldg., Suite 210
16 E. Main Street
Rochester, NY 14614-1803

EXAMINER
BROCK II, PAUL E

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 11/06/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Offic Action Summary	Application No.	Applicant(s)	
	10/039,319	KOCON ET AL.	
	Examiner	Art Unit	
	Paul E Brock II	2815	

-- The MAILING DATE of this communication appears on the cover sheet with th correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 21-39 is/are pending in the application.

4a) Of the above claim(s) 26,29,30,32 and 33 is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 21-25,27,28,31 and 34-39 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 09 November 2001 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 3 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Species 1 depicted in figures 2 – 2d in Paper No. 7 is acknowledged. A quick review of figures 2 – 2d clearly show that claims 26, 29 and 30 are not supported by the elected species. Therefore claims 26, 29 and 30 have been treated as non-elected.

2. Claims 26, 29, 30, 32 and 33 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected species, there being no allowable generic or linking claim. Election was made **without** traverse in Paper No. 7.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the plurality of gate trenches, the first conductivity as N-type and the second conductivity as P-type must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 21 – 25, 27, 28, 31 and 34 – 39 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

6. Claim 21 recites the limitation "said body regions" in 22nd line of the claim. There is insufficient antecedent basis for this limitation in the claim. For purposes of this office action this recitation of "said body regions" will be considered --said well region--.

7. It is not clear in claim 24 how "the upper layer comprises a heavily doped portion of the substrate" while claim 21 claims "forming a doped upper layer on a semiconductor substrate." How can the doped upper layer both be on the substrate and comprise a portion of the substrate?

8. It is not clear in claim 25 what is meant by "wherein one of the source regions is disposed between and adjacent to one of the source regions and a gate trench." How can one of the source regions be disposed between itself and the gate trench? Is the second "one of the source regions" the same as the second recitation of "one of the source regions?

9. Claims 37 and 38 recite the limitations "the first polarization" and "the second polarization" in first and second lines of the claims. There is insufficient antecedent basis for this limitation in the claims. For purposes of this office action "polarization" will be considered --polarity--.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 21, 23 – 25, 27, 28, 31 and 35 – 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harada (USPAT 5298780, Harada) in view of Okabe et al. (USPAT 5877527, Okabe).

With regard to claim 21, Harada discloses in figures 3 – 14 a process for forming an improved trench MOS-gated device. Harada discloses in figure 3 forming a doped upper layer (2) on a semiconductor substrate, the upper layer having an upper surface and an underlying drain region. Harada discloses in figure 4 forming a well region (3) having a first polarity in the upper layer, the well region overlying the drain region. Harada discloses in figure 5 forming a gate trench mask (23) on the upper surface of the upper layer. Harada discloses in figure 6 forming a plurality of gate trenches (40) extending from the upper surface of the upper layer through the well region to the drain region. Harada discloses in figure 7 forming sidewalls and

floor (13) each comprising a dielectric material in each of the gate trenches. Harada discloses in figures 8 – 11 filling each of the gate trenches to a selected level substantially below the upper surface of the upper level with a conductive gate material (4). Harada discloses in figure 7 removing the trench mask from the upper surface of the upper layer. Harada discloses in figure 12 forming an isolation layer (15a) of dielectric material on the upper surface of the upper layer and within the gate trench, the isolation layer overlying the gate material and substantially filling the trench. Harada discloses in figure 13 removing the dielectric layer from the upper surface of the upper layer, the dielectric layer remaining within and substantially filling the trench having an upper surface that is substantially coplanar with the upper surface of the upper layer. Harada discloses in figures 12 – 13 forming a plurality of heavily doped source regions having a second polarity in the well regions, the source regions extending to a selected depth from the upper surface of the upper layer. Harada discloses in figures 14 forming a metal contact (6) to the well and source regions over the upper surface of the upper layer. Harada does not disclose forming a plurality of heavily doped body regions having a first polarity at the upper surface of the upper layer and that the metal contacts make electrical contact to these body regions. Okabe teaches in figure 8 forming a plurality of heavily doped body regions (13a) having a first polarity at an upper surface of an upper layer (3), the body regions overlying a drain region in the upper layer. Okabe further teaches in figure 1 forming a metal contact (14) to the body and source regions (5) over the upper surface of the upper layer. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the heavily doped body regions of Okabe in the method of Harada in order to promote electrical contact between the well regions and the overlying source-body metallization layer.

With regard to claim 23, Harada discloses in figures 3 – 14 and column 4, lines 50 – 53 wherein the upper layer comprises an epitaxial layer.

With regard to claim 24, Harada discloses in figures 3 – 14 wherein the upper layer comprises a heavily doped portion of the substrate.

With regard to claim 25, Harada discloses in figure 14 wherein one of the source regions is disposed between and adjacent to one of the source regions and a gate trench.

With regard to claim 27, Harada discloses in figure 4 and column 4, lines 54 – 57 wherein the forming a well region comprises doping the upper layer.

With regard to claim 28, Okabe teaches in figure 8 wherein the forming heavily doped body regions comprises further doping the upper layer.

With regard to claim 31, Harada does not teach implanting the entire upper surface of the substrate with ions of the second polarity in the forming of the source regions. Okabe teaches in figures 7 – 10 implanting an entire upper surface of the substrate with ions of the second polarity (B), then forming a body mask (24) on the upper surface of the substrate, the mask comprising openings transverse to the trenches. Okabe further teaches in figures 8 and 9 wherein doping the upper surface of the substrate with a dopant of the first polarity, then removing the body mask to form the body regions. It would have been further obvious to one of ordinary skill in the art at the time of the present invention to use the blanket ion deposition of Okabe in the method of forming the source of Harada in order to precisely control the dopant dose of the source region as is well known in the art.

With regard to claim 35, Harada discloses in figure 8 and column 5, lines 10 – 12 wherein the conductive gate material within the gate trench is doped polysilicon.

With regard to claim 36, Harada discloses in figure 14 wherein the selected level of gate material in the trench is substantially coplanar with the selected depth of the source regions in the upper layer.

With regard to claim 37, Harada discloses in figures 4 – 14 wherein the first polarity is P and the second polarity is N.

With regard to claim 38, Harada discloses in figures 4 – 14 and column 6, lines 6 – 10 wherein the first polarization is N and the second polarization is P.

With regard to claim 39, Harada discloses in column 6, lines 6 – 10 wherein the device is a power MOSFET.

12. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Harada and Okabe as applied to claim 21 above, and further in view of Baba et al. (USPAT 5578508, Baba).

With regard to claim 22, it is not clear if Harada and Okabe teach wherein the substrate comprises monocrystalline silicon. Baba teaches in figure 3a and column 5, lines 4 – 8 wherein the substrate (10) comprises monocrystalline silicon. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the substrate of monocrystalline silicon of Baba in the method of Harada and Okabe in order to use a semiconductor substrate with good electrical characteristics.

13. Claim 34 is rejected under 35 U.S.C. 103(a) as being unpatentable over Harada and Okabe as applied to claim 21 above, and further in view of Baliga (USPAT 5323040).

With regard to claim 34, it is not clear if Harada and Okabe teach wherein the dielectric material forming the sidewalls, the floor, and the isolation layer 'in the gate trench comprises silicon dioxide. Baliga teaches in figure 2 and column 1, lines 53 – 66 wherein the dielectric material forming the sidewalls, the floor, and the isolation layer in a gate trench comprises silicon dioxide. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the silicon dioxide of Baliga as the sidewalls, floor and isolation layer of Harada and Okabe in order to easily implement gate drive circuitry as taught by Baliga in column 1, lines 53 – 66.

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Baliga '898, Tomatsu et al., Kato et al., Mo et al., Hshieh et al., Floyd et al., Temple, Yamamoto et al., Brown and Darwish all disclose trench MOSFETS.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E Brock II whose telephone number is (703)308-6236. The examiner can normally be reached on 8:30 AM-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703)308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7722 for regular communications and (703)308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Paul E Brock II
October 29, 2002

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800